

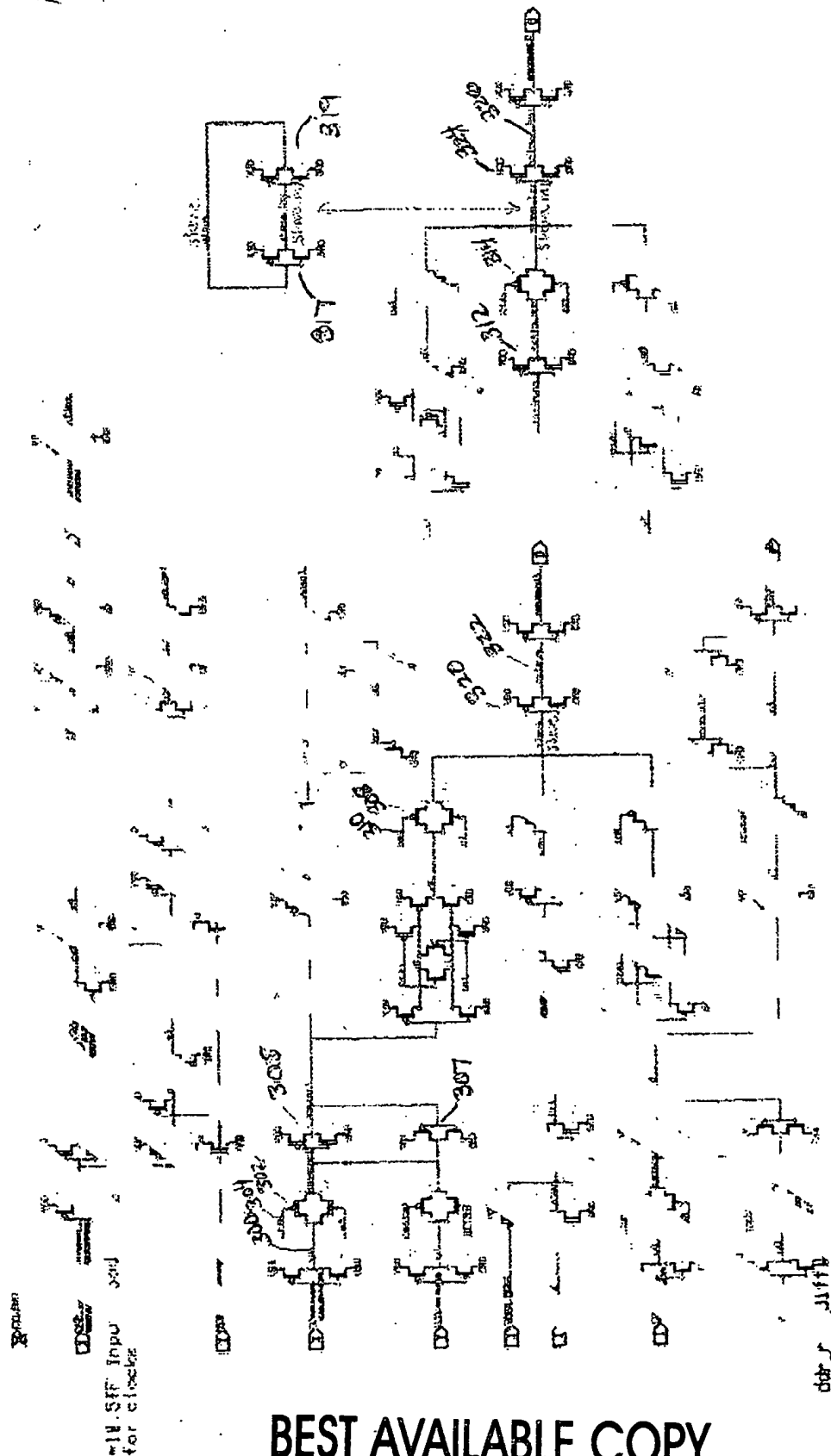
EXHIBIT A

WARNING: This cell is for ddr pads ONLY.
Use elsewhere at your own risk.

ddr_reg_diff1 pad ddr register with differential outputs.

Assumes non-overlapping complementary clocks.
Assumes differential master clocks and standard local clock buffers.
Designed to drive v.ainv.015 load.

DATE: 11/17/05



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